REMARKS/ARGUMENTS

In the Office Action mailed November 21, 2008, claims 1, 3, 4, and 6 – 9 were rejected. Applicant hereby requests reconsideration of the application in view of the below provided remarks. No claims have been amended, canceled, or added.

Response to Claim Rejections

Claims 1, 3, 4, 8, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dedic (U.S. Pat. No. 5,384,570) in view of Applicant's Admitted Prior Art (AAPA), Fig. 2.

Claim 1 recites:

> "A single track-and-hold circuit having an input signal (Vin) and an output signal (Vs), a bootstrap switch (14a) having as its inputs a clock signal and an input signal (vin), said input signal (vin) of said bootstrap switch (14a) being connected to said output signal (Vs) of said circuit via a current source (20) and a buffering transistor (30), characterized in that said input signal (vin) of said bootstrap switch (14a) comprises said output signal (Vs) of said circuit; said single track-and-hold circuit further comprising a capacitor (12), said input signal (Vin) being connected to said capacitor (12) via a switch (10), said switch (10) being closed during a track mode of said circuit and open during a hold mode of said circuit, said bootstrap switch (14a) having as an output to said switch (10), a clock signal (clkboot) equal to said input signal (Vin) added to a supply voltage (Vdd); and
>
> including ***a second bootstrap switch (14b), the input signal (vin) of which is connected to said output signal (Vs) of said single track-and-hold circuit via said current source (20) and said buffering transistor (30) of said single track-and-hold circuit.***" (emphasis added)

As recited in amended claim 1, the first and second bootstrap switches are connected to the output signal (Vs) via the current source (20) and the buffering transistor (30). That is, the first and second bootstrap switches are connected to the output signal (Vs) via the same current source (20) and the same buffering transistor (30).

Applicant asserts that a *prima facie* case of obviousness has not been established with respect to claim 1 because the Office action does not address all of the limitations of claim 1. In particular, the Office action does not address where or how Dedic in view of the AAPA teaches all of the limitations related to the second bootstrap switch (14b).

The Final Office action addresses the limitations of bootstrap switch (14a) as follows:

> "AAPA in Fig. 3 teaches...a bootstrap switch (14a) having as its inputs a clock signal and an input signal (vin);" (emphasis added)
>
> "The combined teachings of Dedic and AAPA further teach said input signal (AAPA, Fig. 3, vin) of said bootstrap switch (AAPA, Fig. 3, 14a) being connected to said output signal (Dedic, Vo) of said circuit via a current source (Dedic, 32) and a buffering transistor (Dedic, 33) characterized in that said input signal (AAPA, Fig. 3 vin) of said bootstrap switch (AAPA, Fig. 3, 14a) comprises said output signal (Dedic, Vo) of said circuit;" (emphasis added)

The Final Office action appears to state that the second bootstrap switch (14b) is taught by AAPA in Fig. 3. The Final Office action addresses the limitations of bootstrap switch (14b) as follows:

> "the input signal (AAPA, Fig. 3, vin) of which is connected to said output signal (Dedic, Vs) of said single track-and-hold circuit via said current source (Dedic, 32) and said buffer transistor (Dedic, 33) of said single track-and-hold circuit." (emphasis added)

Applicant asserts that Dedic does not teach an output signal connected to a second bootstrap switch as recited in claim 1. In particular, the Final Office action cites "Dedic, Vs" as teaching the "of which is connected to said output signal" as recited in claim 1. However, Applicant has not found a teaching in Dedic of a signal "Vs," which represents an output signal or of an output signal that is connected to a second bootstrap switch as recited in claim 1.

Because Dedic does not teach an output signal connected to a second bootstrap switch as recited in claim 1, Applicant asserts that a *prima facie* case of obviousness has not been established.

With respect to Fig. 3 of the AAPA, Applicant points out that Fig. 3 teaches first and second bootstrap switches (14a and 14b), however, neither of the two bootstrap switches have an input signal that is connected to the output signal. In particular, the input (Vin) to the bootstrap switches (14a and 14b) of Fig. 3 is not connected to the output signal (V). While Dedic may teach an output signal connected to one bootstrap switch (see Dedic, Fig. 3), Dedic does not teach or suggest that the same output signal is connected to two bootstrap switches as recited in claim 1.

Additionally, Applicant respectfully points out that VSC1 and VSC2 in Fig. 11 of Dedic represent two separate voltage storage circuits, Dedic col. 25, lines 46 – 48. Although Fig. 11 depicts two bootstrap switched driving devices (4, 5), the two bootstrap switched driving devices (4, 5) are each associated with a different one of the two separate voltage storage devices, VSC1 and VSC2, and with two separate amplifier elements (3). In contrast to Dedic, amended claim 1 recites a single track-and-hold circuit that includes first and second bootstrap switches, where the first and second bootstrap switches are connected to the output signal (Vs) via the same current source and the same buffering transistor. Clearly the two bootstrap switched driving devices (4,5) depicted in Fig. 11 of Dedic are not connected to the output signal via the same amplifier element (3) (where the amplifier element (3) is alleged to include the level shifting and buffering means of claim 1 as previously presented). Because Dedic does not teach first and second bootstrap switches that are connected to an output signal via the same current source and the same buffering transistor, Applicant asserts that amended claim 1 is patentable over Dedic in view of the AAPA.

Dependent Claims 3, 4, and 6 – 9

Claims 3, 4, and 6 – 9 are dependent on claim 1. Applicant respectfully asserts claims 3, 4, and 6 – 9 are allowable at least based on an allowable base claim.

CONCLUSION

Applicant respectfully requests reconsideration of the claims in view of the amendments remarks made herein. A notice of allowance is earnestly solicited.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-4019** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-4019** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Petition is hereby made under 37 C.F.R. 1.136(a) to extend the time for response to the Office Action of 02/21/2009 to and through 03/21/2009, comprising an extension of the shortened statutory period of one month.

Respectfully submitted,

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